All-optical 100-Gbit/s word packet time-division-multiplexed access node in a looped-back configuration: enabling technologies for sequential add–drop functionality

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We experimentally demonstrate the adding, dropping, and passing through of 100-Gbit/s word packets in a looped-back all-optical time-division-multiplexed (TDM) access node. Packets are routed with a 17-dB contrast ratio and demultiplexed with a 20-dB contrast ratio. This node uses short 100-Gbit/s words to demonstrate its potential to process data packets from multiple sources and to perform packet switching in a multinode ring network configuration. The ability to tolerate timing jitter as well as varying input signal characteristics is essential to an all-optical access node in a multinode network. For 2-ps input pulses, the header processor has a timing window of ~5 ps, and the demultiplexer has a timing window of ~5.5 ps. This allows for tolerance to bit-to-bit timing jitters or to an increase in the pulse width of as much as 3 ps. Packet-to-packet timing jitter is detected and compensated by the technique used to synchronize the local source to each packet. The key enabling technologies of an all-optical TDM packet add–drop multiplexer are discussed, including an erbium-doped fiber laser, a nonlinear optical loop mirror logic gate, self-synchronization to incoming packets with a fast-saturation/slow-recovery gain element followed by an intensity discriminator, a two-wavelength nonlinear optical loop mirror demultiplexer, and synchronization of new packets to the network packet rate with a phase-locked loop. The local source is automatically synchronized to the incoming packet, because it uses an extracted pulse from the packet, which has a contrast ratio of >20 dB to the rest of the packet. Finally, new packets are added by use of a local laser and a synchronization method, which gives a timing jitter of ~1 ps. Using a statistical method of measuring Q value with picosecond resolution, we show that a header processor with two cascaded logic gates has a Q value of 7.1 with a 95% confidence level. © 2000 Optical Society of America

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1. All-Optical Packet Time-Division-Multiplexed Network Access

High-speed network access through all-optical time-division-multiplexed (TDM) add–drop multiplexers (ADM's) can help to increase single-channel speeds and network flexibility. TDM network technologies can be advantageous for high-speed networks, because they lead more naturally to packet switching.

Also, the system architecture and protocol can be simplified, since less control is required for one TDM channel than for multiple wavelength-division-multiplexed channels. Applications such as shared memory computing can be simplified, because TDM packets on a single channel arrive in the order in which they were sent out. In addition, TDM technologies complement wavelength-division-multiplexed (WDM) research, since each wavelength channel can be upgraded to higher speeds.

Several TDM network architectures have been proposed and tested. L. P. Barry *et al.* propose a star network design in which a phase-locked-loop is used for clock recovery and electroabsorption modulators are used for the channel drop and the demultiplexing functions.[1] The design for a packet-switched helical local area network structure as well as several key all-optical components has also been developed.[2]

All-optical devices for logic at 100 Gbit/s and rate conversion at 80 Gbit/s have been demonstrated with a single signal source.[3,4] Additionally, a TDM ShuffleNet design, using terahertz optical asymmetric devices for logic switching as well as demultiplexing, has been developed.[5] The ShuffleNet design has been implemented as a packet switching network with a special header coding for routing and demultiplexing with fast tunable delay lines.[6]

Subsystems involving adding and/or dropping have also been demonstrated. The simultaneous add and drop of 40-Gbit/s TDM channels with monolithically integrated Mach–Zehnder interferometers is demonstrated by Jepsen *et al.*[7] Also, electroabsorption modulators have been used in bit-interleaved TDM network ADM's at 40 GHz.[8] The drop function of an access node is demonstrated by Cotter *et al.*, in which packets are routed by extraction of the marker pulse at a different bit period or different polarization.[9] The address recognition is performed by an AND function logic gate with four-wave mixing in a semiconductor laser amplifier.[10] Kamatani *et al.* describe a method of extracting the clock timing with a phase-locked loop based on four-wave mixing in a semiconductor laser amplifier, followed by demultiplexing with four-wave mixing in fiber.[11] Additionally, the interoperability of all-optical devices for the packet-drop functionality has been demonstrated with lasers synchronized through a phase-locked loop.[12] Phase-locked-loop synchronization for header processing of individual packets is not tolerant of the interpacket jitter that may occur as multiple nodes attempt to access the same network. A method of synchronization to incoming packets with no special marker pulses has been proposed,[13] although the output pulses have not been cascaded to other all-optical devices. The interoperability of all-optical nodes within a network, critical to the design and implementation of a network, has not yet been demonstrated.

In this paper we present an ADM composed of all-optical fiber devices. The instantaneous nonlinearities of optical fiber make it a potential candidate for high-speed optical processing. Using 100-Gbit/s words, we demonstrate for the first time to our knowledge both the add and the drop functions controlled by an all-optical header processor, by looping the ADM on itself to form a simple sequential network. The cascading of the ADM functions is a necessary step for demonstrating a multinode all-optical network. That is to say, although dropping and demultiplexing of packets may be demonstrated with one ADM, it is necessary to have a second ADM to drop and demultiplex packets from the first ADM to determine whether the first ADM has successfully added a packet. Among the key necessary technologies is the capability to route and demultiplex on a packet-by-packet basis with tolerance to interpacket jitter, interbit jitter, and varying input pulse characteristics. Such packet-switching technology has the potential to increase network flexibility. The adding, dropping, and passing through of packets is de-

termined by an all-optical header processor, and the reading of the payload bits is performed by an all-optical demultiplexer. Additionally, the current method of sending a long bit pattern through a telecommunication device and counting the number of errors that occur, to measure its performance, is currently limited to ~15 Gbit/s. For testing the reliability of all-optical devices operating at much higher speeds, we demonstrate a method of analysis by looking at the performance of the logic gates used in the header processor.

We use 100-Gbit/s words to show the compatibility of this all-optical packet-TDM demonstration ADM for use in a multinode ring configuration by looping the back-to-the-network port back to the input of the node. The key enabling technologies include transmitters, a header processor, synchronization circuits for individual packets as well as at the average packet rate, and a demultiplexer. The transmitters are passively mode-locked erbium-doped fiber lasers ($\lambda \sim$ 1535–1550 nm, $\Delta\tau \sim$ 1–5 ps) followed by fixed word encoders. The header processor unit is an all-optical low-birefringence (low-bi) nonlinear optical loop mirror logic gate. Self-synchronization to extract a bit from the incoming packet allows the bit to be used as the local source for packet-by-packet synchronization. The self-synchronization unit uses a fast-saturation/slow-recovery gain element followed by an intensity discriminator. All-optical demultiplexing is accomplished with a two-wavelength nonlinear optical loop mirror with high-nonlinearity fiber. And finally, synchronization of new packets to the network packet rate is achieved with a phase-locked loop between the incoming packets and the local transmitter. Packet routing is performed by a commercially available LiNbO$_3$ modulator. Each of these ADM components is individually tested and characterized to confirm its functionality. The output of two cascaded logic gates like the one used in the header processor has a contrast ratio of 10 dB and a statistically determined Q value of 7.1, corresponding to a bit error rate (BER) of 7×10^{-13}. Extraction of the first pulse of incoming packets (for use as the local source) is achieved with a contrast ratio of >20 dB, and synchronization of the local transmitter to the incoming packet gives an interlaser timing jitter of ~1 ps. For the ADM looped back on itself we achieve contrast ratios of 17 dB in the router and 20 dB in the demultiplexer.

This demonstration provides insights into the compatibility issues of several all-optical components. We show that these all-optical components can be brought to function together to perform key ADM functions. For any cascaded function the output pulse characteristics of the first device must be compatible for use as the input pulse of the second device. Conversely, the second device must have some tolerance to varying input pulse characteristics. We also demonstrate the ability to synchronize on a packet-by-packet basis with self-synchronization as well as at the packet repetition rate of the network with a phase-locked-loop. The main challenge to extending
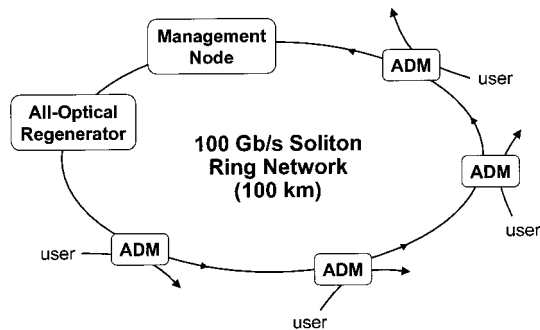
Fig. 1. Schematic of slotted-TDM metropolitan area ring network.
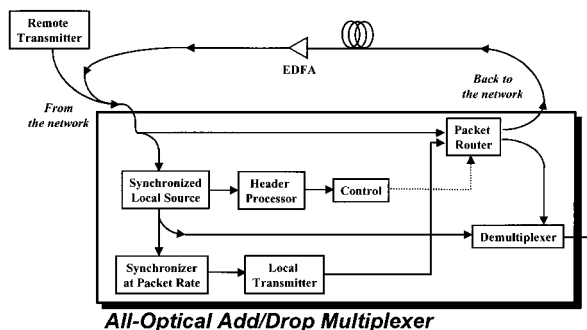

All-Optical Add/Drop Multiplexer

Fig. 2. Schematic diagram of looped-back node. A self-synchronization unit generates the local clock sources used by the header processor and the synchronized local pulse source used by the demultiplexer. The header processor checks the addresses of the incoming packets and determines the direction of the routing. The demultiplexer is used to read the data in the packet. A synchronizer at the packet repetition rate is used to synchronize the local transmitter (new packet generator) to the network. The back-to-the-network port is looped back to the input.

this demonstration to even higher bit rates and/or longer packets is in providing the necessary power levels without degrading the signal-to-noise ratio. High-powered amplifiers with short lengths of highly doped erbium fibers are needed for short-pulse amplification. Amplified spontaneous emission (ASE) and dispersive wave shedding by solitons are the leading causes of signal background and noise. Bandpass filtering is used for limiting the ASE outside the signal wavelength as well as for spectral reshaping of the pulses at various points to compensate for pulse distortions.

In this paper we demonstrate packet add–drop functionality in an all-optical ADM. First, an overview of a potential network architecture is described in Section 2. In Section 3 we discuss the setup and configuration of the looped-back ADM. We show the results of all-optical components integrated into an ADM looped back on itself in Section 4. A performance analysis of the header processor through a statistical method is discussed in Section 5. In Section 6 the key enabling technologies for the ADM are described and the performance of each component is evaluated. Discussion of the challenges of this access node follows in Section 7. Finally, Section 8 summarizes the demonstration.

2. Ring Network Architecture

One possible network architecture that uses the ADM's discussed in this paper is a ring slotted TDM metropolitan area network, shown schematically in Fig. 1. The ADM's allow for access of data packets to the network. Our focus in this paper will be on the demonstration of the ADM and the key enabling technologies necessary for high-speed all-optical TDM networking. A simplistic protocol for address checking is adopted in which, if the address of the incoming packet matches that of the local node, the packet is taken off the network (dropped) and a new packet is allowed onto the network. Otherwise, the incoming packet is allowed to continue on the network. By implementing the access node all optically, we can overcome the bottlenecks of optical–electronic–optical conversions and increase the single-channel speed of TDM networks.

For compatibility with high-speed all-optical pro-

cessing the packet ring architecture has a number of advantages over the bus and star topologies. First, access to the ring network is deterministic, not contention based. By avoiding contention, we reduce the need for optical buffering. Second, the ring's inherent symmetry forms a natural basis for fairness-guarantee mechanisms, which does not become less fair as the geometry is increased. Also, the ring has protective switching capabilities. Moreover, the absence of a central switch permits lower entry cost and ease of expansion. In contrast, a bus is vulnerable to physical damage and has an inherent head-end asymmetry and unfairness. Architectures such as the helical local area network[2] attempt to overcome the limitations of buses, but the three-fiber implementation may be considered to be an inefficient use of resources and still does not guard against physical damage. Star systems are unattractive, because power is distributed among all the nodes, and power is a limited resource at high speeds.

However, the slotted ring does have some drawbacks. First, the average latency is half the ring round-trip time for a unidirectional ring. Second, each node must operate at the aggregate traffic speed rather than at the average speed available to the node. Finally, like a laser, the ring network permits recirculation of noise from previous passes, which requires the use of a management node as well as perhaps all-optical regenerators for system clean up.

When we focus specifically on the ADM's in this ring network, there are several key functions that must be performed by the building blocks of each ADM for multiple ADM's to be able to operate with one another on the network scale. As discussed above, an important first-step demonstration is that of an ADM looped back on itself, which demonstrates the interoperability of the building blocks and both the successful adding and dropping of packets from the network. Figure 2 shows a block diagram of the ADM looped back on itself. A remote transmitter
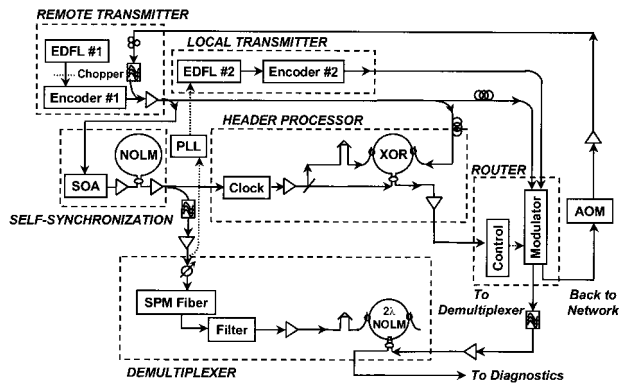
Fig. 3. Experimental setup of access node. PLL, phase-locked-loop; SPM, self-phase modulation. Fixed word encoders create 100-Gbit/s word packets from EDFL's. The NOLM logic gate performs an XOR function to compare the addresses of the incoming packets, and the output triggers the packet router. The 2λ NOLM demultiplexes the individual bits in the packet payload.

generates an incoming packet. The synchronized local source generates the local clock and the local fixed address for the address recognition. The header processor compares the local address to the incoming packet address and the output triggers the packet router. The local transmitter is synchronized to the network packet rate and generates new packets to be added to the network. The demultiplexer bit rate downconverts from the packet bit rate to the packet repetition rate.

3. Setup of Sequential Add–Drop Multiplexer Circuit Demonstration

A more detailed setup of the ADM is shown in Fig. 3. A remote transmitter sends a chopped sequence of packets (packet 1 is 100110 . . .). When the chopper is blocking packet 1, the packets looped back from the packet router (a chopped sequence from the back-to-the-network port) are transmitted. Although both packets are fixed and repetitive, the interleaving of the sequences of packets can be used to simulate instantaneous packet-to-packet changes in content and timing. The packet repetition rate is 21 MHz and is limited by the repetition rate of the erbium-doped fiber lasers (EDFL's). The chopping frequency is 195 Hz, which means that many of the same packets are transmitted for each sequence of packets. However, because the fiber has no memory, receiving the same packet many times should not affect the performance of the header processor or demultiplexer. The self-synchronization unit extracts from the incoming packets a single bit that is used as the local source for the header processor and the demultiplexer. The address of the incoming packet is compared with the local address in the header processor. The output of the header processor is used to control the packet router. If the packet is determined to be for the local node (i.e., addresses match), the packet is routed to the demultiplexer. Otherwise, it is sent back to the network, which in this case again loops back to the input of the node. The de-

multiplexer is used to demonstrate downconversion from the 100-GHz bit rate to the packet rate by extracting individual bits in the payload of the packet. A new packet (pattern 2 is 100100 . . .) may be added by use of a local transmitter that is synchronized to the average packet rate of the network through a phase-locked loop.

A. Devices Outside the Access Node

The components that emulate the network outside the node are the remote transmitter and the back-to-the-network loop back. The transmitter (discussed in detail in Subsection 6.D) consists of an EDFL ($\lambda =$ 1535 nm, $\Delta\tau = 2$ ps) followed by a 100-Gbit/s fixed word encoder. The first three bits are considered to be the address header, and the rest are the data payload. Note that it is not necessary for the data packet to occupy such a small fraction of the data stream. The packet size and rate may both be increased to accommodate more data when implemented in a real network. The spacing between packets must simply be longer than the recovery time of the self-synchronization unit ($\sim$0.5 ns). The back-to-the-network port is looped back to the input of the access node through an acousto-optic modulator (AOM) and a fiber coupler. The AOM is synchronized to the frequency of the chopper at the output of encoder 1. This means that the packets looped back to the input are also a chopped sequence, and proper setting of the phase of the modulation signal ensures that the packets will not collide with the packets from encoder 1.

B. Devices Composing the Access Node

The four main components that make up the local access node are the self-synchronization unit, the header processor, the demultiplexer, and the local transmitter. Each component is discussed in detail in Section 6. At the input to the node, part of the packet energy is tapped for synchronization, part for the header processor to check the address, and the remainder is sent to the modulator to be routed. For header processing we generate a synchronized local clock (111) and a local address (011) for an all-optical logic gate.[14] The output of the header processor is sent to a threshold detector, which generates the control pulse for the packet router.

The self-synchronization unit selects the first pulse from an incoming packet, making it automatically synchronized with the incoming packet.[12] We can treat the first pulse as a marker pulse, although it is optically the same as the other pulses in the packets. First, a transmission function with a fast-saturation/slow-recovery gain medium is imposed across the packet to create higher intensity for the first pulse in the packet. Then the remaining pulses of the packet are removed with an intensity discriminator. Note that the guard time between packets must be longer than the recovery time of the gain element.

The all-optical logic gates used for header processing are realized by use of low-bi nonlinear optical loop mirrors (low-bi NOLM's). The low birefringence is

generated by means of wrapping fibers with low background birefringence on aluminum mandrels. This low birefringence allows the copropagating pulses along orthogonal polarizations in the loop to phase shift through cross-phase modulation and ensures that two pulses have a reasonably long interaction length. The timing window makes the NOLM's tolerant to possible timing jitter between the bits.

The demultiplexer is a two-wavelength (2λ) NOLM[15] using high-nonlinearity fiber. The device uses a control pulse at a different wavelength than that of the incoming signal. By adjusting the relative timing between the control pulse and the signal packet we can select the position within the packet that is to be demultiplexed. The timing window is determined by the group-velocity walk-off between the two wavelengths.

The local transmitter is another EDFL, which is synchronized to the self-synchronization unit output through a phase-locked loop and an AOM–grating pair in the laser,[15] followed by a 100-Gbit/s fixed word encoder. The EDFL is a passively mode-locked Er–Yb-codoped fiber laser in a linear cavity configuration. The fixed word encoder is constructed by fiber couplers and delay lines. A single laser pulse is split into four pulses, each pulse is time delayed with respect to the others, and the pulses are recombined to form the word packet with 10-ps bit-to-bit separation.

4. Experimental Results of Looped Back Add–Drop Multiplexers

In this section we demonstrate the sequential adding and dropping of packets by the ADM. Subsection 4.A focuses on the packet routing of packets from the remote and the local transmitters. When the packet is dropped from the network, it is sent to the demultiplexer, and the demultiplexing results are discussed in Subsection 4.B.

A. Packet Routing

A commercial 2×2 LiNbO$_3$ modulator is used as the packet router. Figures 4(a) and 4(b) show the output of the control unit for the packet router when the address of packets from encoder 1 and 2 are different (i.e., one matches and the other does not match the local address). To switch the packet router, a 6-V control signal is applied to the modulator. The figures indicate that the header processor correctly checks the addresses and triggers the modulator to route the packets appropriately in each case, and the packets are routed on a packet-by-packet basis. For example, in Fig. 4(a), the chopped sequence of packets from encoder 1 trigger the modulator to route each packet back to the network, whereas the interleaved sequence of packets from encoder 2 do not trigger the modulator.

We demonstrate sequential adding, dropping, and passing through of packets from different sources in our access node. Figure 5 shows cross correlations of the outgoing packets at the back-to-the-network port, immediately after the packet router. Figure
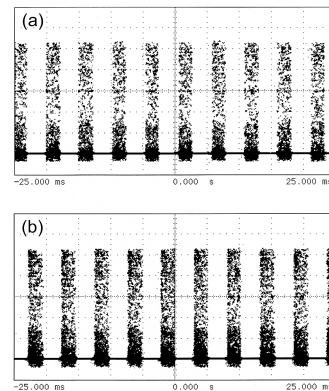

Fig. 4. Digital scope traces of the control signal to the packet router for different address packets. To switch the packet router, a 6-V control signal is needed to drive the modulator. (a) Control signal to modulator when encoder 2 has a matching address and encoder 1 does not have a matching address. (b) Control signal to modulator when encoder 1 has a matching address and encoder 2 does not have a matching address.

5(a) shows that the packet from encoder 1 (100110 . . .) can be passed through (sent back to the network), and Fig. 5(b) shows the case in which the packet is dropped with at least 17-dB contrast ratio. As shown in Fig. 5(c), a new packet (100100 . . .) can be added when the old packet has been dropped. The contrast ratio of the packet routing is limited by the extinction ratio of the LiNbO$_3$ modulator. The figures show that each incoming packet can be correctly routed with the information in the address header without conversion to electronics.

B. Demultiplexing of Bits

Figure 6 shows that, when the address of the incoming packet matches the local address, the demultiplexer can read the bits in the packet. A simplified header (100) is generated by both encoders so that both packets will be routed to the demultiplexer. We show the cross correlation of the incoming packets to the node from encoders 1 and 2 in Figs. 6(a) and 6(e), respectively. In the top panel the payload (110 . . .) of encoder 1 is shown by cross correlation to be demultiplexed [Figs. 6(b)–6(d)]. Likewise, the bottom panel shows the demultiplexed payload of encoder 2 (100 . . .) in Figs. 6(f)–6(h). The bits are individually demultiplexed by means of adjusting the relative timing between the control pulse and the incoming packet. In a real network, N demultiplexers will be necessary for $1/N$ demultiplexing of the entire packet. The energy contrast ratio between the demultiplexed 1 and 0 is at least 20 dB, and the switching energy is less than 1 pJ/pulse. Note that, whereas the input pulse widths of encoder 1 and the demultiplexed bits are approximately the same, this is not the case for encoder 2. This is because the output pulse width is set by a narrow-band (0.9-nm) spectral filter at the output of the demultiplexer. In a real network the demultiplexed bits will be sent to energy detectors and converted to electronic signals,
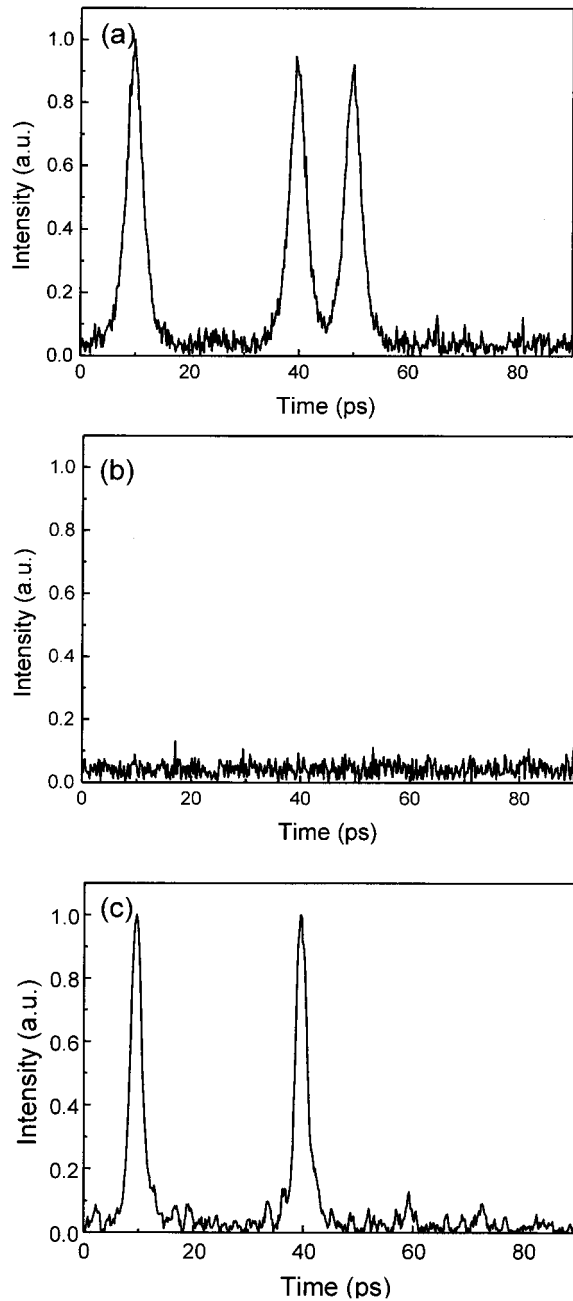
Fig. 5. Cross correlation of packets at the back-to-the-network port immediately after the LiNbO₃ packet router. Depending on the output of the header processor, an incoming packet may be routed back to the network or dropped to the demultiplexer. A new packet may also be added when the incoming packet is dropped. (a) Packet is passed-through (back to the network). (b) Packet is dropped with 17-dB contrast ratio. (c) New packet is added when incoming packet is dropped off the network.

and thus the pulse width may not have much of an effect as long as it is shorter than the bit period. The residue that can be seen in the 0 bit positions is the leakage of the control pulse. This leakage is at a different wavelength than that of the switched-out signal and can be further attenuated with another bandpass filter.
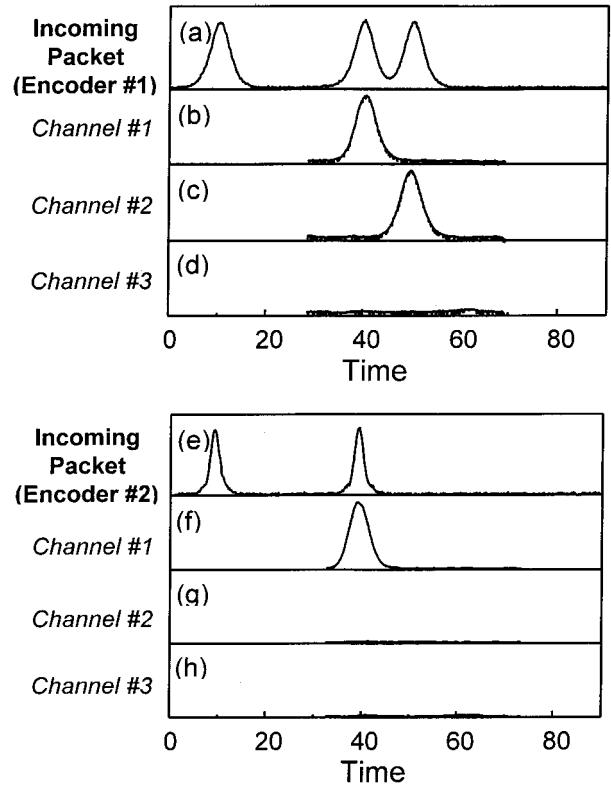

Fig. 6. Cross correlations of incoming packets and demultiplexed bits from the payload at the output of the demultiplexer. The pump leakage, which can be seen as residue in the 0 bit positions, may be attenuated with a bandpass filter. Contrast ratio is >20 dB between the demultiplexed 1's and 0's. (a) Incoming packet from encoder 1. (b)–(d) Demultiplexed payload of encoder 1. (e) Incoming packet from encoder 2. (f)–(h) Demultiplexed payload from encoder 2.

5. *Q*-Value Analysis Technique and Its Application to the Header Processor

New measurement techniques for testing and monitoring the performance of all-optical devices are needed as all-optical telecommunication devices start to push the single-channel speeds toward 100 Gbit/s and beyond. A sampling technique[16,17] using a cross correlator and a reference can be used to perform Q-value analysis of high-speed optical devices. This method allows us to measure eye diagrams with picosecond resolutions. However, the speed of the technique is limited to the sampling speed. This technique has possible applications as a statistical monitor of potential system performance in high-speed optical networks. Although it cannot be used to detect and/or correct specific errors in data packets, the technique gives a statistical Q value from which a BER can be inferred.

To demonstrate this technique, we apply it to an all-optical header processor consisting of two synchronized lasers, 100-Gbit/s fixed word encoders, and two NOLM logic gates. The setup for the logic gates is shown in Fig. 7. This setup is more complex than that shown in Fig. 3 in that it consists of two levels of logic. The first gate, an inverter, checks to see
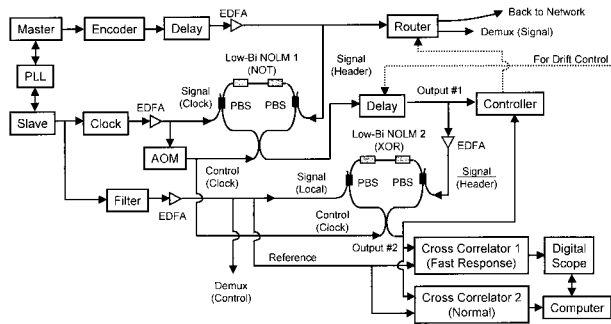
Fig. 7.   Experimental setup of Q-analysis technique.   The master laser passes through the encoder producing 0001011100, and the slave laser passes through the clock producing 111.   The output of the header processor, consisting of two NOLM's, is sent to cross correlator 1 for measuring the eye diagram.   Cross correlator 2 is used for environmental drift control.   PLL, phase-locked-loop; PBS, polarization beam splitter.
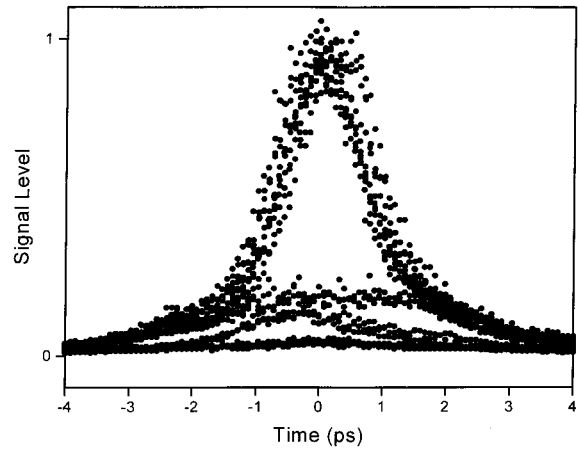

Fig. 8.   Eye diagram of header processor.   This is the trace of the eye diagrams taken with the setup of Fig. 7 where the trace is taken by means of moving an optical delay stage in cross correlator 1.   It is an overlay of all the different possible combinations of the 3-bit incoming header and the two possible values of 0 or 1 for the local bit.

whether the address header is all 1's, indicating an empty packet.   The second gate, an exclusive-OR (XOR), checks to see whether the address matches the local address.   Thus this setup allows for more complete header checking.   Although the implementation of the measurement technique is not dependent on the number of levels of logic, the results show that the overall Q value from a header processor with cascaded logic gates is still acceptable.

The output of the header processor is split and sent to the diagnostics for performance analysis.   Cross correlator 2 is used to control timing drifts caused by thermal fluctuations.   By adjusting the relative timing between the master laser encoder and the slave laser encoder with a variable delay stage, we can obtain any one of eight possible 3-bit patterns.   Cross correlator 1 is slightly modified by use of a fast-response ($\sim$10-ns rise and decay time) photomultiplier tube to remove any averaging effects.   By use of a digital scope to take single-shot scans of the signal from the photomultiplier tube, a single pulse response is taken per scan.   We take a large number of scans while varying the timing between the reference pulse and the output of the header processor.   Then, by overlaying the scans, we can map out the eye diagram with picosecond resolution for all the possible patterns.

The eye diagram for the header processor is shown in Fig. 8.   The eye diagram is for return-to-zero, hyperbolic secant pulses, and it is an overlay of all possible outputs from the header processor.   The input header is equally varied between all the eight possible 3-bit combinations.   The local address is 010, and thus the local address bit may be a 1 or a 0, depending on which bit is scanned.   Because the NOLM has a finite polarization extinction ratio, there is pump leakage present.   Consequently, in the XOR ($\wedge$)gate, the 0 level is different for the case without any pump pulses (i.e., $0 \wedge 0 = 0$) and for the case with two-pump pulses (i.e., $1 \wedge 1 = 0 +$ leakage).   This leads to a spread of the 0 level in the eye diagram.   However, there is no such spread for the 1 level, because the

nonlinear transmission from the NOLM dominates any pump leakage.

By fixing the reference pulse at the center of the bit period we can measure the Q value at the center of the eye opening from which we can statistically calculate the potential BER.   The Q value is defined by $Q = (I_1 - I_0)/(\sigma_1 + \sigma_0)$, with I_1 and I_0 being the sampled means of the ON and the OFF, respectively, and with σ_1 and σ_0 being the sampled standard deviations of the the ON and the OFF, respectively.[18]   The measured Q value is an optical Q where we have neglected the relatively small electronic noise in the photomultiplier tube.   The statistical BER is given by BER $= 0.5 \times \mathrm{erfc}(Q/\sqrt{2})$, where the erfc is the complementary error function.   Note that by sampling in the middle of the eye we are measuring the instantaneous response of the header processor output cross correlated with a reference pulse.   The resolution of the sample is determined by the pulse width of the reference pulse.   Thus the cross-correlation technique takes only one sample point in the bit period but actually integrates the overlapped energy between the signal and the reference.   For each 3-bit pattern, 150 data points are taken.   Because there are eight different possible 3-bit patterns, the total number of data points is 1200.   In addition, because the local bit can be 0 or 1, there are 1200 data points for the 1 level and the 0 level.   With these points we find a Q value of 7.1, which corresponds to a BER of 7.0×10^{-13} for a 12-pJ switching energy.[19]   For one logic gate operation the Q value should be much higher, since the cascading of logic gates tends to degrade the contrast ratio and therefore degrade the Q value.

Because this is a statistical method, we must look at the associated confidence interval to calculate possible errors in the measurement.   The confidence interval is an interval of values that contains the true

value of a parameter with a given confidence level. For a given system the confidence interval for the mean[20] is given by

$$P\left(I_n - t_{n-1,1-\alpha/2}\frac{\sigma_n}{\sqrt{n}} < \mu < I_n + t_{n-1,1-\alpha/2}\frac{\sigma_n}{\sqrt{n}}\right)$$
$$= 1 - \alpha, \quad (1)$$

and the confidence interval for the variance is given by

$$P\left[\frac{(n-1)\sigma_n^2}{\chi_{n-1,1-\alpha/2}^2} < \sigma^2 < \frac{(n-1)\sigma_n^2}{\chi_{n-1,\alpha/2}^2}\right] = 1 - \alpha, \quad (2)$$

where I_n is the sampled mean, μ is the (unknown) true mean, σ is the sampled standard deviation, σ is the (unknown) true standard deviation, n is the number of sampled points, and $(1 - \alpha) \times 100\%$ is the confidence interval level. $t_{v,p}$ and $\chi_{v,p}^2$ are the standard t distribution and the chi-square distribution, respectively, with subscripts being appropriately substituted with the subscripts defined by the confidence intervals. By looking at the confidence interval and setting the confidence level to 95%, we can calculate the error range of the Q value to be from 6.7 to 7.4 for the eye diagram of Fig. 8. This means a worst-case BER of 8.8×10^{-12} and a best-case BER of 4.8×10^{-14}. Note that this error range is inversely related to the number of sample points for a given confidence level.

6. Details of Key Enabling Technologies

In this section we describe the four key enabling technologies of this ADM. Each component is individually tested to demonstrate its functionality. The self-synchronization unit described in Subsection 6.A allows for packet-by-packet timing extraction. Subsection 6.B discusses the header processor, and Subsection 6.C discusses the demultiplexer. Finally, in Subsection 6.D, the local transmitter and synchronization to the packet rate for the adding of new packets are described.

A. Self-Synchronization Unit

In a ring network an incoming packet may be from any of the nodes on the network. When originally added to the network or during propagation, different packets may experience different delays. This introduces an interpacket jitter, which the ADM must be able to tolerate to correctly process the header bits and demultiplex the data payload of each individual packet. Figure 9 shows a schematic diagram for the functional design (i.e., extraction of the packet timing directly from the packet). Data packets begin with a 1 bit, which serves as the marker bit. Note that its temporal, spectral, and polarization characteristics are not distinguished from the rest of the packet. A differential intensity profile is imposed on the incoming packet so that the first bit has a higher intensity than the rest of the packet. Then, an intensity discriminator is used to extract the higher-intensity pulse, which is the marker pulse in this case.
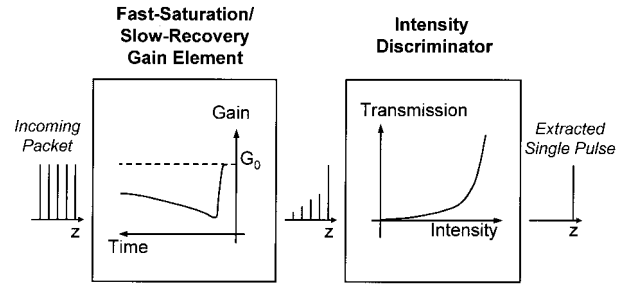

Fig. 9. Schematic diagram of the self-synchronization scheme. It contains two elements: the fast-saturation/slow-recovery gain element and the intensity discriminator. G_0, unsaturated gain.

We demonstrate the self-synchronization unit, using the setup shown in Fig. 10. A 100-Gbit/s word packet is generated by a passively mode-locked fiber laser ($\lambda = 1535$ nm, $\Delta\tau = 1.5$ psec) followed by a fixed word encoder. The data packet is sent to the fast-saturation/slow-recovery gain element to obtain a pulse train with a strong first pulse. Then the output is sent to the intensity discriminator by means of an erbium-doped fiber amplifier (EDFA) to compensate for the 1-dB net insertion loss of the gain element as well as to enhance the energy in the pulses. The energy of the first pulse is 15 pJ at the output of the EDFA.

We choose a semiconductor optical amplifier (SOA) to perform the fast-saturation/slow-recovery transmission function. SOA's have fast gain saturation when excited with short optical pulses, and the saturation can occur during one pulse width for pulses of several picoseconds.[21] The saturated gain of the SOA, however, has a relatively long recovery time, which ranges from 0.2 to 1 ns depending on different SOA's.[22] When we properly set the input power of the optical pulses and bias current of the SOA, only the first pulse in the packet experiences an unsaturated gain. The remaining pulses experience a gain
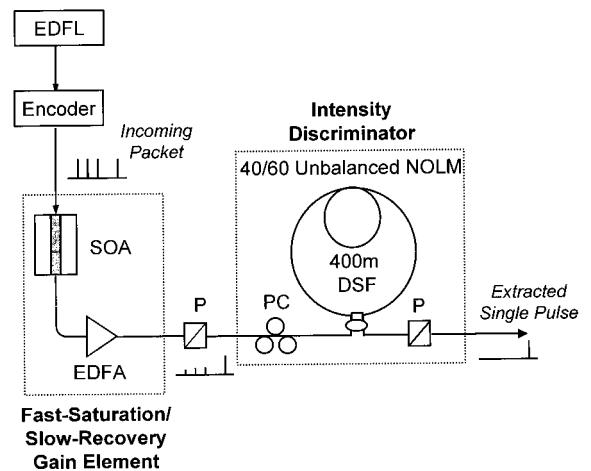

Fig. 10. Experimental setup for self-synchronization. A SOA is used as the fast-saturation/slow-recovery gain element. The intensity discriminator is a 40:60 unbalanced NOLM. PC, polarization controller; P, polarizer; DSF, dispersion-shifted fiber.
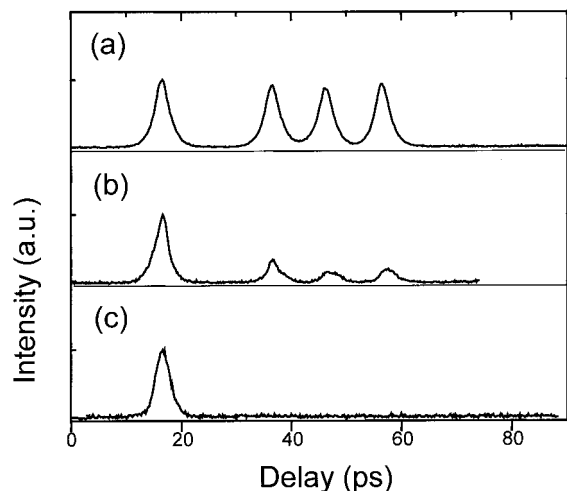
Fig. 11. Cross-correlation results of the self-synchronization scheme. (a) Input data packet. (b) Output data packet from the SOA. (c) Extracted single pulse from the unbalanced loop mirror intensity discriminator. The extracted single pulse has a >20-dB contrast ratio to the rest of the bits in the input packet.
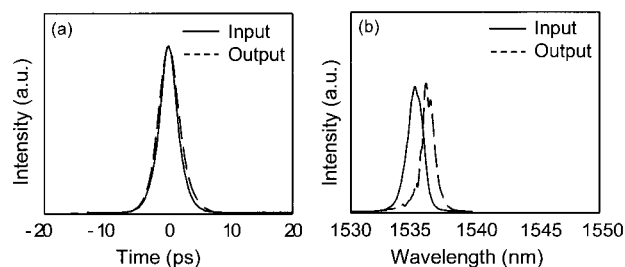

Fig. 12. (a) Autocorrelation and (b) spectra of the extracted pulse from the self-synchronization unit. There is minimal pulse distortion, and the slight wavelength shift is due to gain dispersion in the semiconductor optical amplifier.

saturated by the first pulse. This gain difference causes the first pulse of a transmitted packet to have a greater intensity than the remaining pulses.

An intensity discriminator then selects the first pulse and suppresses the rest, resulting in extraction of a single pulse from the packet. We use the combination of an unbalanced NOLM and a polarizer as the intensity discriminator. The coupler in the loop has an uneven power-splitting ratio of 40:60, and the fiber is a 400-m dispersion-shifted fiber with $\lambda_0 = 1493$ nm. The clockwise and counterclockwise beams in the loop experience different nonlinear phase shifts because of the different input intensities of the pulses. The NOLM can be adjusted so that it has a higher transmission for the high-intensity pulse than for low-intensity pulses. Additionally, since nonlinear polarization rotation induced in the fiber of the loop mirror is also intensity dependent, a polarizer at the output of the loop mirror increases the contrast ratio.

Figure 11 shows the cross correlation at different stages of the self-synchronization unit. Using an input energy of 2 pJ/pulse to saturate the SOA at a current of 50 mA, we obtain an intensity contrast ratio of more than 3 dB between the first pulse and the remaining ones in the packet for a uniform input pulse train [Fig. 11(b)]. The resultant 3-dB contrast ratio is not sensitive to input pulse energy. This intensity contrast is further enhanced to >20 dB after the unbalanced NOLM [Fig. 11(c)] intensity discriminator. With the EDFA between the SOA and the intensity discriminator the overall insertion gain for the first pulse of the packet is 6.5 dB.

The autocorrelation and optical spectra of these extracted single pulses at the output of the self-synchronization setup are illustrated in Fig. 12 and compared with those of the input pulses. It is important to maintain the pulse quality through the

self-synchronization unit, since the extracted pulse will be used as the local source for the header processor and the demultiplexer. A typical phenomenon related to gain saturation in a SOA device leads to a slight frequency shift.[21] The time–bandwidth product of the extracted pulse is 0.34.

This self-synchronization does place some restrictions on the packet frames. It requires a time guard band between packets to be longer than the SOA recovery time. One half the length of time between the end of the self-synchronization recovery time and the nominal start of the packet is the amount of interpacket timing jitter that can be tolerated. Also, if the packets are long, there could be two detrimental effects in the current configuration. The first is if there is a long series of 0's, which will allow the SOA to recover, followed by a 1, which may then be mistaken for the beginning of the next packet. The second is that long packets tend to have much higher average powers, which may damage the SOA device. A possible solution is to add an electronic gate that is turned off after receiving the first extracted pulse and turned on after a fixed packet duration so as to block most of the bits in the packets. Such a gate would thereby ensure that the first pulse of the subsequent packet obtain maximum gain.

B. Header Processor

Incoming packets may also have accumulated interbit jitter within the packet. For the packet header to be processed by logic gates the gates must be designed to have a timing window of approximately half the bit period. In our case the control clock pulses are split by a 50:50 coupler and counter propagate in the NOLM along one axis of the wrapped low-bi fiber. The signals to be compared are coupled into each propagation direction through polarization beam splitters and aligned along the other axis of the fiber. Copropagating control and signal pulses acquire a nonlinear phase shift through cross-phase modulation, and the counter-propagating clock pulses interfere when they recombine at the 50:50 coupler. The NOLM is biased so that, when the two arms are balanced, the clock pulses are reflected. Otherwise, the pulses are transmitted. The walk-off length between orthogonal axes is ~115 m (birefringence, $\Delta n \sim 3 \times 10^{-6}$), and the total length of the fiber is
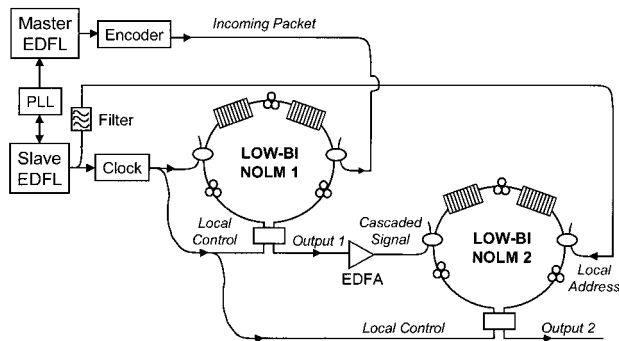
Fig. 13. Experimental setup for demonstration of two cascaded logic gates. PLL, phase-locked loop.
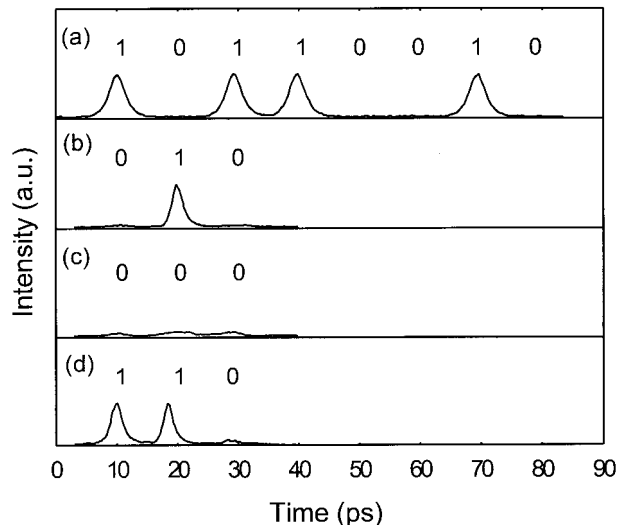

Fig. 14. Cross correlation results of the header processor. (a) Input data packet. (b) Output of the inverter. (c) Output at the XOR gate when the headers match. (d) Output at the XOR gate when the headers do not match (the inverted incoming header is 010, and the local header is 100).

~300 m. Thus rotating the polarization axis after each walk-off length gives measured timing windows of ~5 ps for 2-ps pulses. The high extinction ratio between the orthogonal polarizations (~40:1) helps to maintain a good output contrast ratio. The logic gates have switching energies of 10 pJ/pulse for nonlinear transmissions of 50%.[14]

To demonstrate the functionality of these logic gates, we implement an inverter gate followed by an XOR gate, as shown in Fig. 13. This is a more complex header processor than that used in the ADM demonstration, in which we use only one gate (XOR) for comparing the incoming address with the local address. Note that the low-bi NOLM logic gates are cascadable and Boolean complete. The sources for the header processor are the master laser representing a transmitter and the slave laser acting as the local laser. They are synchronized with a phase-locked loop. Both lasers produce 2-ps pulses at 1535 nm. A 2.3-nm bandpass filter spectrally shapes the slave laser pulse used as the local address bit, making the pulse closer to transform limited. The output from the master laser passes through a fixed word encoder to produce the packet pattern 0001011100. Similarly, the output from the slave laser passes through the clock generator to produce the 3-bit pattern 111. The inverter determines whether the incoming packet address is all 1's, corresponding to the special case for an empty packet, and the XOR gate determines whether the addresses match. When the packet is empty, the output of the first gate is 000. Likewise, when the addresses match, the output of the second gate is 000. We use a threshold detector to distinguish these two cases from the not-empty and unmatched cases, which have at least one 1 in the output.

The header processor output is detailed in Fig. 14. The data packet including the header is given in Fig. 14(a), whereas the inverted header output from the inverter, which is used as the input of the second logic gate (XOR), is given in Fig. 14(b). The XOR gate output when the header matches (no match) the local header is given in Fig. 14(c) [14(d)]. The ON–OFF contrast ratio after the cascaded gates is 10 dB. The contrast ratio is limited by pulse distortion from the EDFA's, which leads to incomplete switching through degradation of the polarization extinction ratio.

The length of the address can readily be scaled up, since the logic gate performs a bit-by-bit comparison. Because the logic gate is Boolean complete and cascadable, even though one gate compares just one address at a time, several cascaded gates can create multiple levels of logic, which may be used to recognize more than one address.

C. Demultiplexer

The 2λ NOLM employed for demultiplexing uses a local control pulse at a different wavelength from the incoming packet. The incoming signal is split by a 50:50 coupler and counter propagated through the NOLM. The second wavelength (control) is coupled in through a WDM, and the control and signal propagate through each other, owing to the difference in group-velocity dispersion. Through cross-phase modulation between different wavelengths a nonlinear phase shift is imposed on the signal pulse that is to be demultiplexed. When the counter-propagating pulses recombine at the 50:50 coupler, the signal pulse with the induced phase shift is transmitted while the rest of the packet is reflected. Whereas the low-bi NOLM's are designed to work for a single wavelength, the 2λ-NOLM could be designed to work for any of a range of signal wavelengths, because the walk-off is determined by the dispersion of the fiber. In our case we also lower the required switching energy to less than 1 pJ/pulse by using high-nonlinearity fiber. The fiber has a smaller core size (effective area $A_{\text{eff}} \sim 16.5~\mu\text{m}^2$ for increased optical intensity as compared with normal dispersion-shifted fiber with $A_{\text{eff}} \sim 50~\mu\text{m}^2$). The germanium doping is also increased to increase the intrinsic nonlinear co-
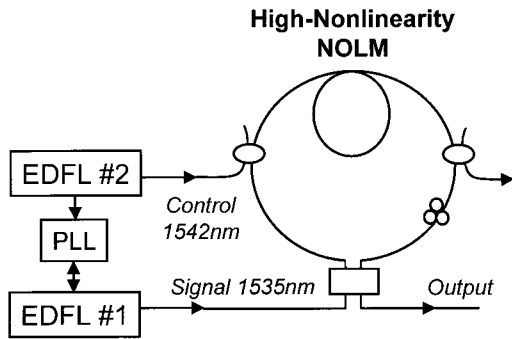
Fig. 15. Experimental setup for 2λ-NOLM demonstration. The high-nonlinearity fiber has a length of 1.64 km, $\lambda_0 = 1530.5$ nm, and a nonlinearity ~4.5 times that of normal dispersion-shifted fibers. zemEDFL 1 ($\lambda = 1535$ nm) and EDFL 2 ($\lambda = 1542$ nm) are synchronized with a phase-locked loop (PLL).

Fig. 17. Autocorrelation of the 2λ-NOLM input and output pulses. Note that there is minimal pulse distortion through the device.

efficient. The effective nonlinearity is 4.5 times that of a normal dispersion-shifted fiber.

The experimental setup for demonstration of the 2λ NOLM is shown in Fig. 15. The device consists of a 50:50 fiber coupler for signal input–output, two WDM couplers for add–drop of the control pulses, and high-nonlinearity fiber. The WDM couplers are periodic with a spacing of ~7.5 nm. One laser provides signal pulses at 1535 nm ($\Delta\tau = 2$ ps) while a second synchronized laser provides control pulses at 1542 nm ($\Delta\tau = 0.8$ ps). The timing tolerance of the 2λ NOLM relies on the wavelength-dependent group-velocity dispersion, and the high-nonlinearity fiber is designed with a dispersion of 0.51 ps/nm/km ($\lambda_0 \sim$ 1530.5 nm, $L \sim 1.65$ km) to yield a measured timing window of ~5.5 ps for this setup.

To characterize this device, we measure the timing window, the switching energy, the nonlinear transmission, and the contrast ratio. The timing window is repeatedly measured at various switching energy levels. At a switching energy of 0.8 pJ/pulse the timing window is nearly square [Fig. 16(a)]. Above this energy the timing window remains squarely shaped with the width increasing to 7 ps at 1.2 pJ/pulse. Using the same data, we observe that the nonlinear transmission increases linearly with the
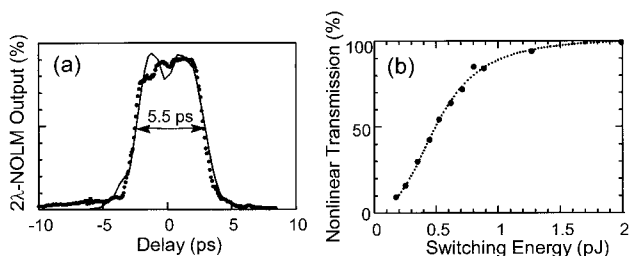

Fig. 16. (a) Switching timing window 2λ NOLM measured at 0.8-pJ/pulse switching energy. Circles, experimental data; solid curve, simulated result based on the nonlinear Schrödinger equation without inclusion of timing jitter. (b) Nonlinear transmission of the 2λ NOLM measured as a function of switching energy. At a switching energy of 0.8 pJ/pulse, the nonlinear transmission is 90%.

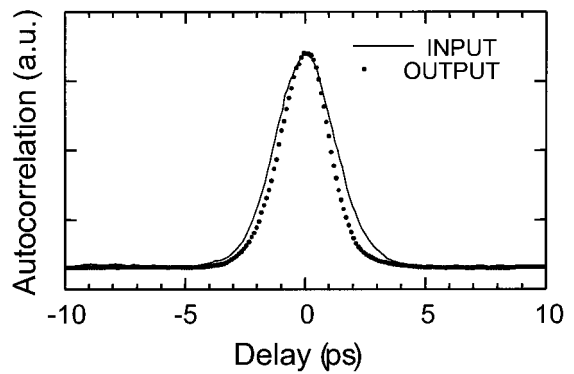switching energy below 0.8 pJ/pulse, as expected [Fig. 16(b)]. At a switching energy of 0.8 pJ/pulse the nonlinear transmission reaches ~90%, implying a phase shift of nearly π in the signal pulse. At higher pulse energies self-phase modulation of the control pulse causes spectral broadening and leakage through the WDM. Because of this leakage the intensity measured at the output port remains nearly constant instead of decreasing sinusoidally. The contrast ratio, measured at 0.8 pJ/pulse switching energy, is 20 dB for signal pulse energies less than 0.5 pJ.

To ensure the pulse quality of the 2λ-NOLM output pulse, we measure the autocorrelation and optical spectra of the output pulse and compare them with the input. For switching energy below 1 pJ/pulse and signal pulse energy below 0.5 pJ, the autocorrelation shows that there is negligible pulse distortion (Fig. 17). For switching energy above 1 pJ/pulse, strong leakage from both signal and control pulses to the output port leads to severe degradation of the 2λ NOLM.

To estimate how timing jitter affects the performance of the 2λ NOLM, we compare the experimental data with computer simulations in which the timing jitter is not included. The simulation is based on the well-known nonlinear Schrödinger equation. For the timing window [Fig. 16(a)], the data also agree well with the simulation except for the small dip in the middle of the timing window. Note that this dip is only ~2 ps wide, implying that it is caused by the presence of timing jitter (see Subsection 6.D for a discussion on the synchronization method).

For the looped-back node demonstration we use part of the extracted single bit from the self-synchronization unit to generate the second (control) wavelength. By propagating the pulse through 400 m of high-nonlinearity fiber with $\lambda_0 = 1534$ nm, we broaden the spectrum through self-phase modulation. Then we use a 2-nm bandpass filter to select the wavelength at 1542 nm for use as the control pulse. This automatically synchronized control
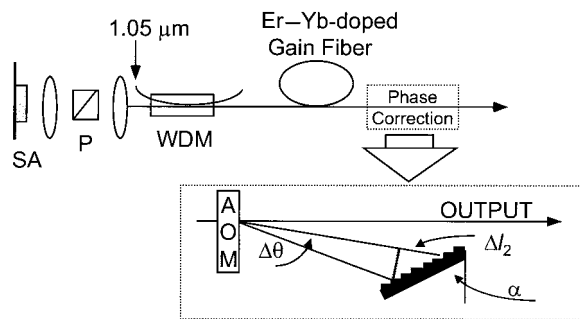
Fig. 18. Schematic of Er–Yb-doped fiber laser configuration. The dashed box shows the phase correction setup. SA, saturable absorber; P, polarizer.
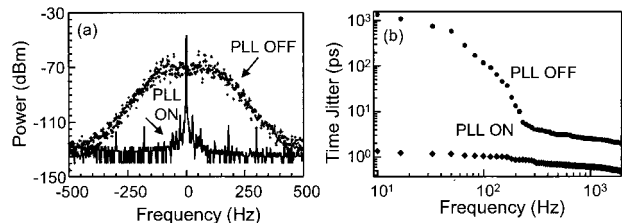

Fig. 19. (a) Power spectra measured at the tenth harmonic of the laser fundamental. (b) Timing jitter of the laser calculated from the power spectra. PLL OFF indicates when the laser is free running, and PLL ON indicates when the laser is synchronized to an electronic synthesizer.

pulse should reduce the detrimental effects of timing jitter on the 2λ NOLM.

D. Local Transmitter

The linear cavity Er–Yb-codoped fiber laser is passively mode locked by a semiconductor saturable absorber, as shown in Fig. 18. The 1.05-μm pump beam from a diode-pumped Nd:YLF laser is introduced by means of a WDM coupler. The WDM coupler has one port spliced to a 1.2-m Er–Yb-codoped gain fiber, whose cleaved end may serve as the laser output coupler. The beam from the other port of the WDM is collimated and focused on the semiconductor saturable absorber, which is mounted directly on the high reflector. The phase correction is achieved by use of an AOM–grating scheme[15] depicted in the dashed box of Fig. 18. The wavelength can be tuned from 1535 to 1550 nm, and the pulse width can be varied from 1 to 5 ps depending on the wavelength, pump power, and cavity loss. In our case, we use $\lambda \sim 1535$ nm and $\Delta\tau \sim 2.3$ ps.

To add new packets to the network, the local transmitter should be synchronized to the packet rate of the network. Although self-synchronization is necessary to find the exact timing of each packet to process the packets from the network with interpacket jitter, it is not necessary to replace packets with such precision. Thus we use a phase-locked-loop scheme to synchronize a local laser to the average incoming packet rate.

The phase-locked loop using the AOM–grating for phase correction works as follows. The output from the gain fiber end (angle cleaved to prevent reflection) is separated into two parts by the AOM. The nondeflected zeroth-order beam serves as the laser output. The deflected first-order beam is reflected by a grating, which is set at an angle (α) to give good reflection as well as sufficient cavity tuning. The AOM deflection angle (θ), proportional to the carrier frequency, varies with the error signal sent to the AOM driver. The change in the AOM deflection angle induces two additive effects in the cavity length: First, a change of the first-order beam angle modifies the wavelength selected by the grating according to $\Delta\lambda = (\lambda \times \Delta\theta)/\tan(\alpha)$; hence the effective cavity length is adjusted through the fiber dispersion.

More dominantly, the variation of the deflection direction gives a physical change in the optical path with $\Delta l_2 = (l \times \Delta\theta)\tan(\alpha)$, where l is the distance between the AOM and the grating. The values of l and α are chosen to achieve sufficient cavity length tuning, limited wavelength fluctuation, and good coupling to the gain fiber. For example, with $l = 25$ cm and $\alpha = 26.7$ deg, a change of 1 MHz in AOM drive frequency results in $\Delta l_2 = 80$ μm and $\Delta\lambda = 1.9$ nm. The physical change Δl_2 provides more than 85% of the 1-kHz change in the repetition rate measured by a spectrum analyzer. Under normal operation conditions of the phase-locked loop the AOM needs to be tuned only approximately a couple of tens of kilohertz, and the wavelength fluctuation in the slave laser is less than 0.005 nm.

By measuring the radio-frequency power spectrum at the local laser fundamental frequency and at a sufficiently high harmonic (N) we can extract the timing jitter. The power spectra contains information about the amplitude as well as phase noise with the relative importance of the phase noise increasing as N^2.[15] The timing jitter of the free-running lasers is first studied to determine the tuning range and the bandwidth of the phase-locked loop required for synchronizing the lasers. We measure the power spectrum at the first and the tenth harmonics [a typical example is shown in Fig. 19(a)] and calculate the timing jitter according to the standard technique, which is discussed in detail in Ref. 14. For the free-running laser [PLL OFF in Fig. 19(b)], the timing jitter is of the order of 1 ps for frequencies above 2 kHz. However, the low-frequency jitter can be orders of magnitude larger, mainly owing to pump power fluctuations, mode beating noise, thermal fluctuations, and mechanical vibrations. This noise characteristic is typical in a passively mode-locked laser: The timing jitter between adjacent pulses is inconsequential, yet the jitter accumulated over a long period can be significantly large. Hence an effective phase-locked loop requires a high temporal resolution for detecting the phase mismatch but relatively low bandwidth for tracking those fluctuations as long as the tuning range is sufficiently large to correct the timing jitter accumulated over the period. The AOM–grating scheme makes the synchronization of the two fiber lasers possible.
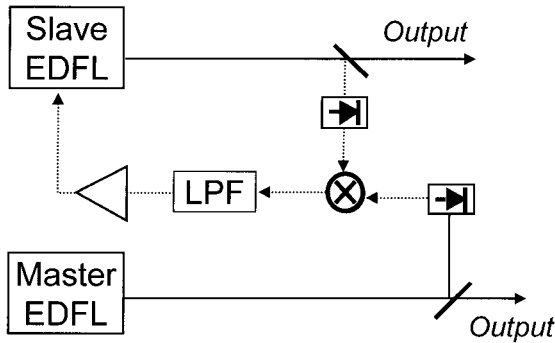
Fig. 20. Schematic diagram of phase error detection. Solid lines, optical paths; dotted lines, electronic circuits. LPF, low-pass filter.

The phase mismatch between the two pulse series is obtained by direct detection. As shown in Fig. 20, each laser has a part of the beam (~2%) sent to a fast detector (response time, ~100 ps) whose output is amplified. The phase mismatch is detected by a radio-frequency mixer, passed through a low-pass filter, and amplified. This error signal is then sent to control a signal generator, which drives the AOM placed inside the slave laser. With this simple direct detection method we find that an EDFL can be well locked to an electronic synthesizer with a timing jitter of approximately 2 ps [PLL ON in Fig. 19(b)]. The result is achieved by means of locking the laser to its fourth harmonic, the highest possible from our synthesizer, to enhance the phase sensitivity of the phase-locked loop. However, when the synthesizer is replaced with a free-running EDFL, we synchronize with the 25th harmonic and achieve an interlaser timing jitter of ~1 ps. We use the cross correlation of the lasers to determine the timing jitter.[15] For simplification we assume that both lasers have Gaussian pulses and that the timing jitter experiences a Gaussian distribution. Then FWHM of the cross-correlation profile can be approximated as $\Delta_x = [(\Delta_1)^2 + (\Delta_1)^2 + J^2]^{1/2}$, where J is the mean square root of the timing jitter and $\Delta_{1,2}$ are the FWHM of the autocorrelation of the lasers.

By using a higher harmonic we reduce the effect of amplitude fluctuations in the error signal. However, precautions must be taken, since there are N locking points representing fixed yet different phases during a fundamental period of the laser. When the phase-locked-loop is turned on, the two lasers are locked to an arbitrary one of the N equivalent locking points. If the timing jitter of the laser (slow drift or sudden spur) is sufficiently large, the phase-locked loop may jump between the different locking points. In this case, the two EDFL's are no longer locked to a determined phase even though the error signal stays near zero. For our EDFL with 2–3% amplitude fluctuation we find that the phase-locked loop works best for $N = 25$ considering both the phase sensitivity and the long-term stability.

7. Discussion

Among the challenges that need to be addressed in a high-speed TDM network is the ability of local nodes to process incoming data from various locations quickly and reliably. By processing data all optically we remove the bottlenecks associated with conversion from optics to electronics and back to optics again. However, this introduces new challenges in terms of synchronization (bit to bit as well as packet to packet). Additionally, whereas electronic detection systems are concerned only with total energy, there is now a strong dependence on pulse shape and intensity. These new challenges are accentuated as the number of nodes on the network increases. In Subsection 7.A we discuss how this ADM demonstration overcomes some of the challenges of multiuser access to the network. Subsection 7.B contains further discussion regarding the extension of this ADM to higher packet rates.

A. Multiuser Access to Network

The results of the looped-back ADM show the potential of this access node to overcome system degradations caused by timing jitter and varying pulse characteristics of incoming packets from a multinode network. The self-synchronization unit is tolerant to interpacket jitter, which may occur as different nodes at different locations attempt to access the same network. Uneven input levels require the bias of the SOA to be set low enough to accept the low signals. All the higher-level signals should be clamped by the SOA gain. Because the packets are from different sources and propagate through different paths, the NOLM logic gate must be tolerant of the different pulse qualities. The header processor has been shown to operate on individual packets independent of the packet source. The timing windows of the header processor and the demultiplexer compensate for bit-to-bit jitter within each packet.

After the header processor it is also necessary to set the bias of the energy detector to distinguish between the matched and unmatched cases for all input packets. Additionally, the threshold level must be set to tolerate output signal fluctuations, which may be as high as ±15%, owing to interference between the logic gate control leakage and the output signal. This interference may be reduced by means of increasing the extinction ratio of the logic gate.

B. Extension to Higher Packet Rate

One major challenge to increasing this demonstration to longer and more closely spaced packets is in achieving the power levels within the node that are needed to switch the logic gates. The research with high-nonlinearity fiber in the demultiplexer implies that specialty fibers can be used to lower the switching energy and thus the power requirements for the node. At a pulse energy of 1 pJ/pulse and a bit rate of 100 Gbit/s the average power necessary from an amplifier is of the order of 100 mW, which is well within the range of commercially available amplifi-

ers. This will help lower the levels of ASE and minimize pulse distortions through amplifiers.

Another source of degradation is from the amplifiers for the data packets. Both ASE and breakup of the pulse due to the necessarily high amplification levels cause degradation of the signal-to-noise ratio. Dispersive waves and ASE background accumulate after several amplifiers. We currently use short-length, high-gain, erbium-doped fiber amplifiers as well as spectral filters to minimize the ASE and re-shape the spectrum of the pulses. For the future there have been promising technological advances in the area of large-area-fiber amplifiers, which aim to minimize nonlinear pulse distortions by lowering the peak intensity within the fiber.[23]

8. Conclusion

A. Integration Results

In conclusion, the main functions of an all-optical packet TDM access node in a looped-back configuration have been demonstrated. This configuration emulates a ring network with at least one other node and is the simplest sequential circuit using the access nodes. The add function involves generating a new packet, which is switched onto the network when an incoming packet is removed. Erbium-doped fiber lasers followed by fixed word encoders are used to generate new packets. The drop function requires address checking in the header processor with a synchronized local source, routing of the incoming packet either to the local node or to the network, and demultiplexing of the packet payload. The contrast ratio for dropping a packet from the network with a $LiNbO_3$ modulator is 17 dB. The payload of the dropped packet is demultiplexed by a 2λ NOLM with a 20-dB contrast ratio. The system is not severely degraded by interpacket jitter, which is compensated for by the self-synchronization unit, or by interbit jitter, which is absorbed by the timing windows of the NOLM's. This demonstration shows that the ADM is capable of being cascaded to form a high-speed multinode ring network because of its ability to process and route data packets all optically.

We find that the necessary high power levels make the system difficult to set up and maintain. ASE and pulse distortions through high-powered amplifiers degrade the signal-to-noise ratio. The use of bandpass filters as well as high-powered, short-length, amplifiers help to eliminate some of the background noise. Energy detectors are carefully set to distinguish between different cases, since background noise not only raises the 0 levels but also gives fluctuations to the 1 levels through interference. For the future the use of high-nonlinearity fibers and new amplifier technologies show great promise in lowering switching energies and providing undistorted amplification. By lowering the energy requirements and improving the amplification process, extension of the system to higher packet rates will be possible.

B. Statistical Performance Analysis

A method of statistically determining the Q value of a 100-Gbit/s system has been presented. As an example we look at the output of two cascaded low-bi NOLM logic gates. We determined the Q value to be 7.1 with a confidence level of 95%. This corresponds to a BER range from 4.8×10^{-14} to 8.8×10^{-12}. The main source of Q-value degradation is from the leakage of the signals, which raises the levels of the 0's. This method can also be applied to other high-speed optical devices as well as to the entire node for monitoring of the system performance.

C. Key Enabling Components

The self-synchronization unit extracts the first pulse from the incoming packet to generate an automatically synchronized local source. A SOA acts as a fast-saturation/slow-recovery element, which imposes an intensity differential across an incoming packet. Then a 40:60 unbalanced NOLM and polarizer act as an intensity discriminator to extract the highest-intensity pulse (the first pulse) and reject the lower-intensity pulses. The contrast ratio of the first pulse to the rest of the packet is >20 dB. With input pulse energies of 2 pJ and a current of 50 mA for the SOA the overall unit has an insertion gain of 6.5 dB for the first pulse. The output pulses are nearly transform limited ($\Delta\tau\Delta\nu \sim 0.34$) with a slight shift in the center wavelength.

Packet-by-packet header processing is achieved with a low-bi NOLM logic gate (contrast ratio, 10 dB). A birefringence of $\Delta n \sim 3 \times 10^{-6}$ is achieved by means of wrapping fiber with low background birefringence on aluminum mandrels. The walk-off between the control and signal polarizations is determined by the birefringence of the fiber. We demonstrate the header processing unit and the cascadability and Boolean completeness of the logic gates by testing an inverter gate and an XOR gate, cascaded together. The timing windows for the gates are ~5 ps for 2-ps pulses. The polarization extinction ratio is at least 40:1. Nonlinear transmission of 50% is achieved for a switching energy of 10 pJ/pulse.

However, the switching energy is only 0.8 pJ/pulse for 90% nonlinear transmission, owing to the 1.65 km of high-nonlinearity fiber in the 2λ-NOLM demultiplexer. The high-nonlinearity fiber has an effective nonlinearity of ~4.5 times that of normal dispersion-shifted fiber. The 2λ NOLM has a switching window of ~5.5 ps for 2-ps pulses and a contrast ratio of 20 dB. In this case the walk-off between the control and signal wavelengths is due to the group-velocity dispersion of the fiber.

The local transmitter is an Er–Yb-codoped linear cavity fiber laser, modified by an AOM and grating, followed by a 100-Gbit/s fixed word encoder. A phase-locked loop provides the error signal between the local laser and the incoming packet rate. The error signal is used to drive the AOM, which deflects the first-order beam accordingly. The first-order

beam is reflected by the grating and forms one end of the laser cavity. Thus the deflection by the AOM changes the overall cavity length. The zeroth-order beam is used as the output of the laser source. By using the 25th harmonic of the fundamental packet repetition rate frequencies, we can extract the phase noise between the two lasers and synchronize to a timing jitter of ~1 ps. The fixed word encoders are formed by means of splitting the laser pulse with a 1×4 coupler, time delaying each pulse with respect to the others by propagating through different lengths of fiber and then recombining the pulses with a 4×1 coupler.

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